Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

**2 S3**

**3 D3**

**4 D1**

**5 S1**

**6 IN1**

**7 GND**

**8 V-**

**9 IN2**

**10 S2**

**11 D2**

**12 D4**

**13 S4**

**14 V+ (Substrate)**

**.088”**

**.087”**

**3**

**4**

**5**

**2 14 13**

**12**

**11**

**10**

**6 7 8 9**

**DIE ID**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .087” X .088” DATE: 11/22/16**

**MFG: SILICONIX THICKNESS .014” P/N: DG303A**

**DG 10.1.2**

#### Rev B, 7/19/02